Solution Overview
Project started as my Ph.D. work

- Czech Technical University in Prague, Faculty of Information Technology
- CESNET (Czech Educational and Scientific NETwork)

Ecosystem includes:

1. Compiler from P4 to VHDL
2. General design of P4 ready NIC (P4NIC)
3. Library for device configuration (lib4dev)
4. Support of the pipeline in PI library (P4Runtime)

We provide all parts required for rapid development

The solution is capable to reach high-speeds

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Solution Overview

1) p4lang/PI Project https://github.com/p4lang/PI

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Architecture of P4 Pipeline
1. **IPv4 Filter** — filtering of packets is based (IPv4 address), the non-IP traffic is dropped
2. **IPv4+IPv6 Filter** — extends the IPv4 Filter with support of IPv6 protocol
3. **Full Filter** — extends the IPv4+IPv6 Filter with support of tagging (VLAN and MPLS)

<table>
<thead>
<tr>
<th>Project</th>
<th>P4 lines</th>
<th>Time [s]</th>
<th>Generated lines</th>
<th>Total lines</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPv4 Filter</td>
<td>91</td>
<td>1.574</td>
<td>6283</td>
<td>24791</td>
</tr>
<tr>
<td>IPv4+IPv6 Filter</td>
<td>129</td>
<td>1.818</td>
<td>9888</td>
<td>28396</td>
</tr>
<tr>
<td>Full Filter</td>
<td>212</td>
<td>1.929</td>
<td>13824</td>
<td>32332</td>
</tr>
</tbody>
</table>

- **Generated lines** — expresses the effort of the generator
- **Total Lines** — the sum of generated lines and lines of library source code (FIFO, TCAM, and so on)
Throughput of test line is 100Gbps
Inefficiency is caused by the *Deparser* block.

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Size and Throughput IV

- Slice Logic = LUTs + Registers

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Compiler and Development Process
Currently supports P4\textsubscript{14}

- P4-HLIR, implemented in Python
- Version with P4C frontend is under development

Generated VHDL code is platform independent

Supported FPGAs

- Xilinx – Virtex 7, Virtex UltraScale+
- Intel

\[
P4 \xrightarrow{P4\text{-to-VHDL}} \text{VHDL} \xrightarrow{Synthesis} \text{bitstream}
\]

No additional tool is needed

- \textit{p4fpga} – requires Bluespec compiler
Each generated pipeline has a different structure
- Keys structure, set of actions, number of tables
- DT = DeviceTree
  - Data structure for hardware description
  - https://www.devicetree.org/

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- Fast HW without comfort control == useless
- Multiplatform library in C language
  - Configuration M+A Tables with rules
  - Device control (Enable/Disable, Reset, etc.)
- No recompilation is needed for new P4 program
- All necessary data are stored in DT on a device
  - Structure of the P4 pipeline
  - Action name ➞ opcode
  - Table name ➞ address space offset
  - Structure of table search key
  - Structure of the pipeline’s address space
- Allows fast and easy development

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- **P4NIC = NIC with P4 generated cores**
  - Basic infrastructure for transfers from/to SW to Ethernet/DMA
  - Doesn’t need to be modified because interface is sustained
  - Used for fast development of P4 accelerated applications

- **Supported cards:**
  - COMBO-100G (Virtex 7, 100 Gbps)
  - COMBO-100G2Q (Virtex 7, 100 Gbps)
  - COMBO-200G2QL (Virtex US+, 2 × 100 Gbps)
Coloured parts are generated by the compiler

White parts stay unchanged

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INT Demo

- P4 Workshop 2017, CA, USA

- INT Sink at 100 Gbps using a single FPGA

- GUI - Flowmon Collector
  - Professional tool for flow monitoring
  - Extended to display delays of switches in INT network

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Open vSwitch (OVS) Acceleration

- Demonstrated on several conferences
  - P4 Workshop 2018, CA, USA
  - TNC18, Trondheim, Norway

- Partial OVS acceleration
  - Input traffic is parsed and assigned with Mark ID
  - Mark ID assignment is configured via DPDK’s RTE Flow

- Accelerated version - 2× higher packet rate

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Service Function Chaining

- P4 Workshop 2018, CA, USA
- Realization of NFV (Network Function Virtualization)
- Implemented using the IPv6 Segment routing
- Capable to process data at 100 Gbps

IPv7 Demo

- FPL 2017, Ghent, Belgium
- Accelerated decapsulation from non-existing IP protocol
- Capable to process data at 100 Gbps
- Demonstration of the project translation (live)

- Demonstration of OVS Acceleration (video)
Future Work and Conclusion
Conclusion

- Full P4 environment for rapid development
  - P4 compiler, configuratin layer, initial FPGA design (P4NIC), build system
- Capable to reach high-speeds (100 Gbps)
- More information about generated pipeline
  - Ph.D. Thesis: *Generation of High-Speed Network Device from High-Level Description*
- Future Work:
  - Remove all bottlenecks from the design
  - Full support of P4_{16}
  - Implementation of verification environment for generated RTLs

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Thank you for your attention.

www.liberouter.org