Server Chiplet Networking

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Abstract

Emerging chiplet-based server platforms and the resulting server chiplet networking present a fundamental shift in the (intra-)host network. Unlike conventional monolithic servers, compute chiplets, I/O chiplets, off-chip memory, and peripheral devices communicate through a collection of heterogeneous interconnects and links, formalizing a new server chiplet network substrate that has not been explored before. This paper makes an initial step by characterizing two generations of AMD EPYC chiplet servers, identifying four communication idiosyncrasies, and summarizing the design implications. We outline some future directions under server chiplet networking and discuss how to build next-generation server systems and applications.

CCS Concepts

• **Computer systems organization → Interconnection architectures**; • **Hardware → Network on chip**; • **Networks → Network performance analysis**.

Keywords

Chiplet, Network on chip, Performance analysis, Host network

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1 Introduction

Chiplet [33, 37, 64, 89, 90, 96] is an emerging semiconductor technology and has garnered significant attention in industry and academia. By dividing monolithic large chips into domain-specific, small, modular dies and composing them via silicon interposers, chiplets drastically improve the wafer yield rate, reduce manufacturing costs, expedite time-to-market, facilitate flexible and scalable hardware innovations, and enable energy- and cost-efficient application specialization. The past few years have seen a number of chiplet-based processors [10, 11, 17, 57, 61, 85, 86], domain-specific hardware accelerators [15, 28, 87], and I/O devices [34, 68, 69].

Commodity servers are increasingly built using chiplets. A server SoC (system-on-chip) consists of several compute and I/O chiplets, connected via specialized on-chip load-store interconnects. A compute chiplet encompasses a few to dozens of cores, sometimes organized as sub-chiplets, sharing per-chiplet last-level cache slices. An I/O chiplet, enclosing a network-on-chip (NoC), provides high-bandwidth and low-latency network connectivity for the memory subsystem and I/O devices. As such, a new type of host network–where we term it **Server Chiplet Networking**–emerges, which serves as the communication subsystem underlying the server SoC.

Server chiplet networking is essentially a network of heterogeneous networks, usually organized into three layers. The physical layer encompasses several different links, such as on-chip cache-coherent interconnects (like AMD Infinity Fabric [3] and UCIe [18]), off-chip memory interconnects, and peripheral I/O buses. The data link layer is a reliable and hierarchical packet-switched network whose topology hinges on the NoC of an I/O chiplet. The transaction layer provides communication semantics and deterministically routes data FLITs from the source to the destination. *Server chiplet networking entails communication characteristics that are drastically different from those of a traditional monolithic SoC, an area that has not been previously explored.*

This paper makes the first step by systematically characterizing two generations of AMD EPYC chiplet servers (§3). We identify four unique aspects of server chiplet networking, i.e., extended data paths with more latency hops, heterogeneous bandwidth domains, inconsistent bandwidth-delay products, and sender-driven aggressive bandwidth partitioning, and discuss the design implications. We believe a networking stack and corresponding ecosystem centered around chiplet networking are strongly needed, and will offer several benefits, including improved communication, greater efficiency, maximized computing usage, and enhanced development capabilities. We conclude the paper by outlining future research directions with some proposals (§4).

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2 Background and Motivation

This section provides some necessary background on chiplets, describes the chiplet-based server SoC (system-on-chip) architecture, and introduces server chiplet networking.

2.1 Chiplet and Why

Chiplet [33, 37, 64, 89, 90, 96], an emerging semiconductor technology, has become a predominant approach to building chips. A chiplet is a discrete and unpackaged modular die that implements specific functionalities, such as processors, memory controllers, I/O subsystems, and acceleration kernels. It provides standardized operating interfaces and is integrated into a compatible 2.5D/3D silicon interposer [99, 100]. The interposer, acting as a bridge, facilitates low-latency and high-speed die-to-die data transfers via specialized chiplet interconnects, such as UCIe [18], BoW [74], and OpenHBI [73]. Today, we have seen several chiplet-based computing products designed, manufactured, and deployed, such as AMD EPYC [10, 11, 57, 58, 85, 86], Intel Xeon Scalable Processor [56, 59, 91], AWS Graviton [61], Ampere AmpereOne [17], NVIDIA H100/H200 [15, 28], and AMD MI300 [87].

Chiplets impose several benefits. First, they improve the yield rate by breaking a large chip into smaller dies, as the defect probability increases with the die size. Considering a standard $360mm^2$ sized wafer and a typical die-yielding model [58, 98], a 4-chiplet ($99mm^2$) design can achieve a yield rate of 37%, doubling that of a monolithic approach (15%). Such improvements become more significant under small process nodes (like 3/5nm). Second, chiplets can be fabricated with different process nodes and foundries, and reused across different hardware substrates, drastically minimizing the time-to-market and reducing the manufacturing cost. Third, they make building flexible and scalable heterogeneous SoCs possible, enabling fast innovation and agility based on the application demands. For example, the recent Intel SDV (software-defined vehicle) SoC [34] employs a multi-node chiplet solution that allows automakers to tailor compute, graphics, and AI capabilities flexibly. Fourth, designers can explore application specialization, apply a Lego-style strategy to design complex SoCs, and freely upgrade/add/drop new functionalities, maximizing the power density and energy efficiency. The Cadence Allegro X platform [12] leverages this for advanced IC packaging design.

2.2 Chiplet-based Server SoC

Most recent server processors are developed using chiplets. Take the AMD EPYC 7302 processor as an example (others are similar). As shown in Figure 1, the server SoC has (a) four compute chiplets or Core Complex Die (CCD) in the AMD terminology and (b) one I/O chiplet. A compute chiplet contains several sub-chiplets (2 in our example) or

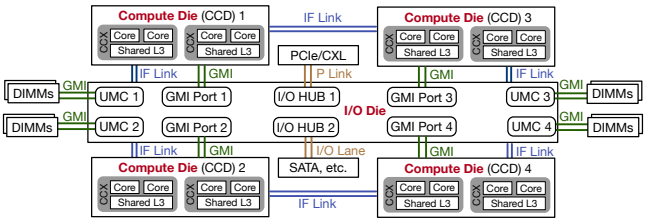


Figure 1: An architecture overview of a chiplet-based server SoC. We take the AMD EPYC processor as an example. CCD = Core Complex Die. GMI=Global Memory Interconnect. IF=Infinity Fabric. UMC=Unified Memory Controller.

Parameters	EPYC 7302	EPYC 9634
Microarchitecture	Zen 2	Zen 4
L1 (per core)	32KB	64KB
L2 (per core)	512KB	1MB
L3 (per CPU)	128MB	384MB
Core#/CCX#/CCD# (per CPU)	16/8/4	84/12/12
Compute Chiplets # (per CPU)	4	12
Process technology (Compute Die)	7nm	5nm
I/O Chiplets # (per CPU)	1	1
Process technology (I/O Die)	12nm	6nm
PCIe Gen/Lane #	Gen4/128	Gen5/128
Base/Turbo Frequency	3/3.3 GHz	2.25/3.7 GHz

Table 1: HW specifications of our two evaluated processors.

Core Complex (CCX) that share the last-level cache slices. A CCX consists of one to dozens of cores, each of which has its own L1 and L2 caches. An I/O chiplet encompasses (a) UMCs (unified memory controllers) that connect to off-chip DIMMs; (b) I/O hubs that provide peripheral links for devices, such as P Links to fast PCIe/CXL slots and I/O lanes to slow SATA-like buses; (c) GMI (global memory interconnect) ports for compute chiplets to access memory; and (d) a mesh network that interconnects different components through some proprietary routing protocols. Compute-Compute and Compute-I/O chiplets talk to each other via the AMD Infinity Fabric or other specialized interconnects like UCIe [18]. Off-chip DIMMs also attach to UMCs through GMI links.

Table 1 presents two AMD EPYC chiplet processors we studied in this paper. Note that the 7302 CPU contains two CCXs per CCD, while the 9634 processor only has one.

2.3 Server Chiplet Networking

Server chiplet networking is the communication subsystem underlying the server SoC that connects different microarchitectural modules and devices. Its physical (*L1*) layer is an agglomeration of on-chip interconnects, off-chip memory links, and peripheral I/O buses, providing connectivity for data flows traversing compute chiplets, I/O chiplets, and devices. Next, the link (*L2*) layer is a reliable and hierarchical packet-switched network. As shown in Figure 2, the first level is the network-on-chip (NoC) in an I/O chiplet, employing a Mesh [31], Torus [55], Cube [25], or Dragonfly [38]

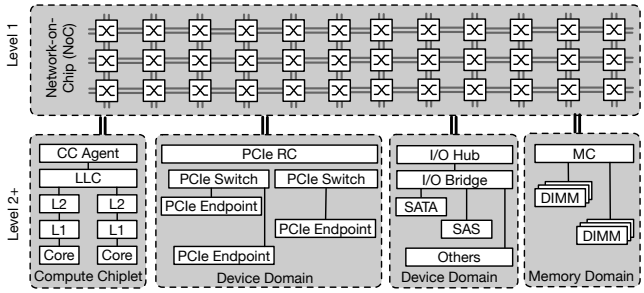


Figure 2: A topological view of server chiplet networking.

topology. The following levels are organized in different compute chiplets or device domains, usually presenting a tree topology. The network contains different switches or routers that use either bufferless or buffered routing protocols. Last, the transaction (*L3*) layer describes data flows from source to destination entities at the cacheline or FLIT granularity, depending on the underlying link. For example, a cacheline-sized LLC snooping request mostly traverses the Infinity Fabric, while a `CXL.mem` transaction, encoded as the FLIT size (68/256B), goes from a compute chiplet and I/O chiplet to a CXL DIMM through an IF, a P Link, and a CXL lane.

Server chiplet networking has become crucial given (a) the proliferation of dense and heterogeneous hardware-accelerated computing boxes [23, 24, 62, 63], (b) increasing interconnect speeds for fast cross-device (domain) data movements [3, 18], and (c) skyrocketing application demands [50]. A new networking stack and corresponding ecosystem (including libraries, utilities, and runtime) are strongly needed, offering several benefits. First, it provides the opportunity to maximize the communication performance under today's sub-microsecond and terabit regime, which is notoriously challenging [4, 40]. Second, it can improve the overall system energy efficiency by accelerating data transfer and streamlining computation-communication overlapping close to the underlying hardware tiers. Third, it facilitates the system's compute, memory, and I/O scalability, avoids superfluous scaling bottlenecks (due to contention and head-of-line blocking), and ameliorates the multi-tenancy support under massive intra-server data flows. Fourth, it enables microscopic per-request and per-flow observability for system diagnostics, anomaly detection, performance profiling, and upper-layer development. **However, our community lacks such a system layer and the capabilities it would provide.**

3 Understanding Server Chiplet Networking

We systematically characterize server chiplet networking, report our findings, and discuss the design implications.

		EPYC 7302	EPYC 9634
Compute Chiplet	L1	1.24 ns	1.19 ns
	L2	5.66 ns	7.51 ns
	L3	34.3 ns	40.8 ns
	Max CCX Q	30 ns	20 ns
	Max CCD Q	20 ns	N/A
I/O Chiplet	Switching Hop	~8 ns	~4 ns
	I/O Hub	~15 ns	~15 ns
Memory/Device	Near	124 ns	141 ns
	Vertical	131 ns	145 ns
	Horizontal	141 ns	150 ns
	Diagonal	145 ns	149 ns
	CXL DIMM	N/A	243 ns

Table 2: The data path latency breakdown. We measured the latency by configuring the pointer-chasing mode of our utility and gradually increasing the working set. We changed the NPS (Node per Socket) configurations and issued memory requests to DIMMs at different positions.

3.1 Experimental Methodology

We use two types of commodity servers for the characterization experiments. The Dell 7525 2U box contains two EPYC 7302 processors and 256GB DDR4. The Supermicro 1U server has one EPYC 9634 processor, 1TB DDR5, and four Micron CZ120 CXL modules (256GB each). Both servers run Ubuntu 22.04. We developed a micro benchmark utility (like others [6]) that can flexibly generate different data flows (such as one or multiple concurrent cachelines, random/sequential read/write access patterns, and temporal or non-temporal writes) over a size-configurable working set, originating from and destined to compute chiplets, memory domains, and device domains across the chiplet networking subsystem. We mostly use latency and bandwidth as performance metrics.

3.2 Extended Data Path with More Latency Hops

Server chiplets add more intermediate hops compared with monolithic ones, increasing the data communication path and incurring some latency overhead. Within a compute (sub)-chiplet, there is a traffic control module that limits the number of outstanding requests. It employs a queueless structure (like Phantom Queue [1]) and uses tokens and back-pressure for overload control. We observe up to 50ns and 20ns queueing delay in an EPYC 7302 and EPYC 9634 processor (Table 2). Inside an I/O chiplet, requests traverse through a sequence of micro-architectural modules before reaching the target DIMM/device (Figure 2), including a cache-coherent master (CCM), several I/O chiplet switching hops (SHops), an I/O hub, a coherent station (CS), and a unified memory controller (UMC). The switching hop and I/O hub take roughly 8ns and 15ns on the EPYC 7302 (4ns and 15ns in the EPYC 9634). Thus, accessing a DIMM at a near, vertical, horizontal, and diagonal position (relative to the compute chiplet) yields different latencies, i.e., 124ns (141ns), 131ns (145ns), 141ns (150ns), and 145ns (149ns) on an EPYC 7302 (9634), because

	To DIMM Read/Write (GB/s)		To CXL Read/Write (GB/s)	
	EPYC 7302	EPYC 9634	EPYC 7302	EPYC 9634
From Core	14.9/3.6	14.6/3.3	N/A	5.4/2.8
From CCX	25.1/7.1	35.2/23.8		23.6/15.8
From CCD	32.5/14.3			
From CPU	106.7/55.1	366.2/270.6		88.1/87.7

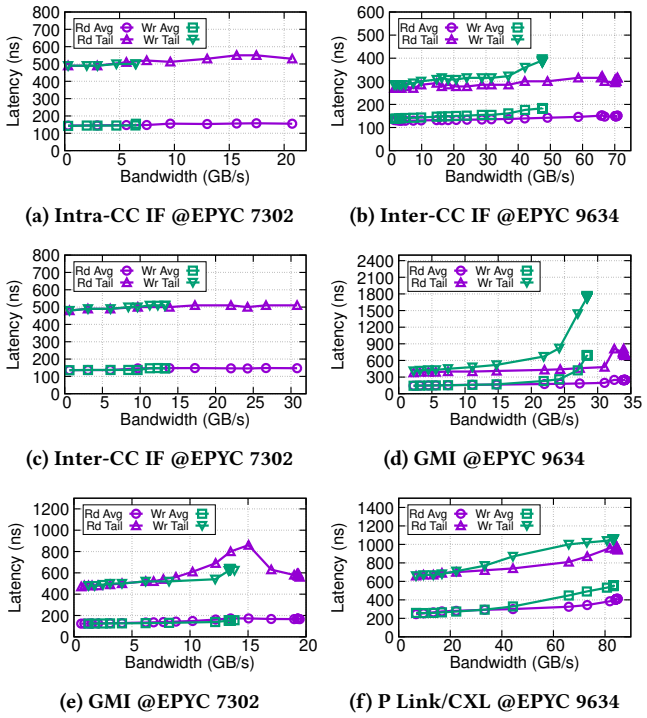
Table 3: Maximum achieved bandwidth from a core/CCX/CCD/CPU when accessing the DIMMs and CXL device. We measured the bandwidth using AVX512 memory read and non-temporal write operations.

the number of traversed hops varies. Accessing a PCIe device not only goes through the I/O hub, but also passes through a PCIe root complex, an I/O moderator (like an I/O northbridge), and P Links. Hence, a cacheline-sized CXL memory access on the EPYC 9634 takes 243ns.

Implication #1: Chiplet servers generally extend the data access path among cores, DIMMs, and devices because of intra/inter-chiplet routing, imposing higher memory and I/O stall cycles. It will affect traditional memory-sensitive primitives, such as memory fences, synchronization locks, and MMIOs. We would also see more granular non-uniform memory access, such as the Sub-NUMA Clustering feature. Asynchronous threading/coroutines, wait-free/lock-free data structures, and locality-aware data placement are becoming much more favorable to elude superfluous memory stalls and maximize core utilization. Recent work on memory-bound stall cycle harvesting [49] is also promising.

3.3 Heterogeneous Bandwidth Domains

Server chiplet networking is an agglomeration of heterogeneous networks that feature different bandwidth domains. The achieved bandwidth is determined by the number of concurrent transactions issued end-to-end over the underlying links, including Infinity Fabric (IF), Global Memory Interconnect (GMI), I/O chiplet internal interconnect, P link, and PCIe/CXL. As shown in Table 3, a core sustains a read/write bandwidth of 14.9/3.6 GB/s and 14.6/3.3 GB/s to DIMMs on an EPYC 7302 and 9634 CPU, respectively, limited by the per-core memory-level parallelism. When using all cores on a compute chiplet, memory read/write bandwidths reach up to 32.5/14.3 GB/s and 35.2/23.8 GB/s, respectively, constrained by the compute chiplet's GMI link capacity. Given that a unified memory controller (UMC) can deliver at most 21.1/19.0 GB/s and 34.9/28.3 GB/s of read/write bandwidth, a compute chiplet must access multiple memory controllers to attain higher aggregated bandwidth. We then activate all 4 and 12 compute chiplets in the two CPUs and issue as many memory accesses as possible to all DIMMs. An EPYC 7302 achieves a peak read/write throughput of 106.7/55.1 GB/s, and an EPYC 9634 attains up to 366.2/270.6 GB/s, both limited by the NoC routing capacity in the I/O chiplet.



(a) Intra-CC IF @EPYC 7302 (b) Inter-CC IF @EPYC 9634

(c) Inter-CC IF @EPYC 7302 (d) GMI @EPYC 9634

(e) GMI @EPYC 7302 (f) P Link/CXL @EPYC 9634

Figure 3: We report the average and tail (P999) latency when varying the bandwidth of the Infinity Fabric (IF), Global Memory Interconnect (GMI), and P Link/CXL on the EPYC 7302 and 9634 processors. We vary the traffic load by issuing sequential read and non-temporal write operations and use `NOP` instructions to control the rate. CC=Compute Chiplet.

Further, when accessing a peripheral device, the I/O path segment (like the I/O hub, P link, and PCIe lanes) can become a bottleneck. For example, on an EPYC 9634, a single core, a single compute chiplet, and all 12 chiplets reach 5.4/2.8 GB/s, 23.6/15.8 GB/s, and 88.1/87.7 GB/s of CXL memory read/write bandwidth, respectively, which is 63.0%/22.2%, 33.0%/33.6%, and 78.1%/69.3% lower than the local DIMM performance due to the high access latency and PCIe/CXL bandwidth limit.

Implication #2: Memory wall [65, 66] is a well-known problem that denotes the bandwidth gap between computing engines and memory subsystems. In chiplet server systems, an emerging hidden "interconnect wall" would happen either within or across chiplets, limiting the data movement speed even before saturating the memory bandwidth. The issue would become common in high-bandwidth servers with terabit I/Os. Thus, being aware of end-to-end bandwidth domains, identifying the bandwidth throttling path segment at runtime, and developing an intra-server traffic matrix [51, 92] are essential for maximizing the data transmission performance. Besides, we expect that more new computational devices that support near-data computing [79, 82, 94] and

distributed and collaborative computing [7, 22, 46] will be designed and implemented.

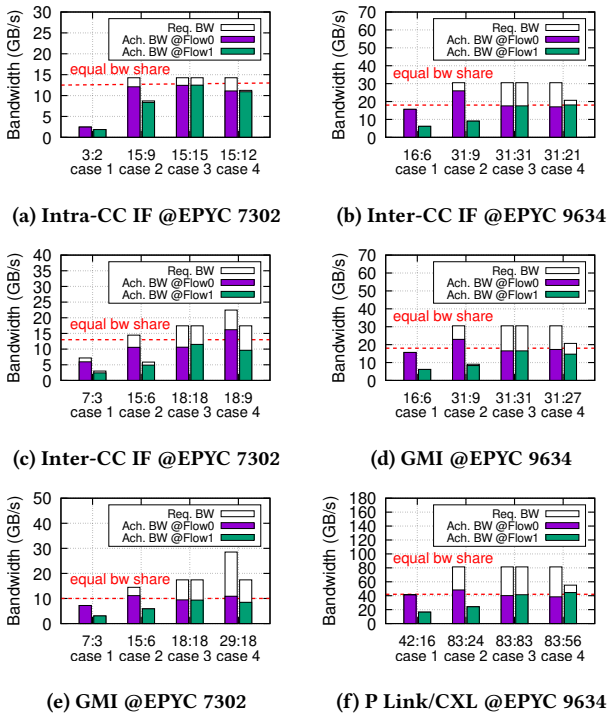
3.4 Inconsistent Bandwidth-Delay Product (BDP)

Memory and I/O requests in chiplet servers traverse several different interconnects with incongruent BDPs. When the number of in-flight transactions exceeds the underlying link bandwidth capacity, one sees queuing or back-pressure overheads, yielding head-of-line blocking. Figure 3 presents our characterizations of different interconnects. Regarding Infinity Fabric, the EPYC 7302 CPU provisions enough bandwidth for intra- and inter-compute chiplet scenarios (Figures-3-a/c). Thus, the average/tail read and write latencies are 144.5ns/490.0ns and 142.5ns/500.0ns, regardless of the load. However, the EPYC 9634 is less-provisioned, where one compute chiplet contains 7 cores, and we see a 2× latency increase when approaching the max bandwidth (Figure 3-b). In terms of GMI, since it connects on-chip memory controllers to off-chip DIMMs through an I/O chiplet, the per-GMI channel bandwidth is less than the on-chip interconnect, causing significant request buffering. As shown in Figures 3-d/e, the memory read average/tail latencies of an EPYC 7302 (9634) rise to 172.5ns/800.0ns (249.5ns/810.2ns) from 123.7ns/470.0ns (143.7ns/380.0ns), respectively. And the write ones increase from 123.9ns/480.0ns (144.1ns/350.2ns) to 153.5ns/630.0ns (695.8ns/1749.8ns). The problem also happens with the P Link/CXL. Since the I/O chiplet on an EPYC 9634 is capable of driving 366.2/270.6 GB/s read/write traffic (Table 3), we observe 1.7/1.4× and 2.1/1.6× average/tail read and write latency increases (Figure 3-f), respectively.

Implication #3: Compared with conventional monolithic servers, chiplet servers generally embody a much larger BDP for data transmission among CPUs, DIMMs, and devices, and can handle more outstanding transactions. However, inconsistent BDP of different links would then incur queuing and head-of-line blocking, jeopardizing bandwidth usage and wasting computing cycles. Dynamic monitoring end-to-end runtime BDP and using it for traffic control becomes vital in server chiplet networking. Akin to rate limiters and traffic policers in today's OS networking and I/O stacks [32, 39, 77, 80], we expect such designs will also be developed and applied to inter-/intra- chiplet communications.

3.5 Sender-driven Aggressive Bandwidth Partitioning

Next, we examine how bandwidth is partitioned in server chiplet networking. We launch two competing flows at different links, use `NOP` instructions to control their requested bandwidth, and see how much bandwidth each flow achieves. When the link is under-subscribed, as expected, both flows



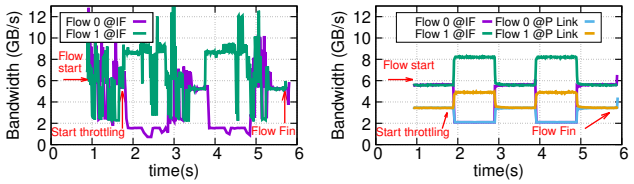
(a) Intra-CC IF @EPYC 7302 (b) Inter-CC IF @EPYC 9634

(c) Inter-CC IF @EPYC 7302 (d) GMI @EPYC 9634

(e) GMI @EPYC 7302 (f) P Link/CXL @EPYC 9634

Figure 4: Bandwidth (BW) partitioning of two competing data flows at a shared link on the EPYC 7302 and 9634 processors. We examine four cases. The first targets when the aggregated requested bandwidth is less than the link capacity, while the other three consider the over-subscription scenario. Case 2 has one flow whose requested bandwidth is less than the equal share. In cases 3 and 4, two flows request the same and different amounts of bandwidth (more than their equal share), respectively. CC=Compute Chiplet.

can receive the requested bandwidth, regardless of the link type (case 1 in Figure 4). When the link is over-subscribed, i.e., the aggregated requested bandwidth exceeds the bandwidth capacity, we find that the bandwidth partition follows a sender-driven aggressive manner (cases 2 and 4). In particular, the flow with a higher demand takes more bandwidth than its equal share. This is because each communication intermediate point at a compute or I/O chiplet is unaware of (a) what a flow is and (b) what the demand of a flow is. As a result, such traffic-oblivious routing always benefits an aggressive sender that pushes more requests in-flight. Two flows with the same demand receive the equilibrium bandwidth (case 3). Further, we evaluate the link bandwidth usage when its housed flows have unsteady demands. Specifically, as shown in Figure 5, we reduce the traffic rate of flow 0 by 2.0GB/s at the 2–3s and 4–5s periods, and observe that flow 1 can reliably take the unused bandwidth at the IF and P Link on an EPYC 9634 processor. However, the EPYC 7302 sees drastic variation at the IF link (we suspect this is due to the



(a) EPYC 7302 (b) EPYC 9634

Figure 5: Bandwidth utilization of two competing flows with fluctuating demands. We throttle flow 0 and see whether flow 1 (unthrottled) can reap the unused bandwidth.

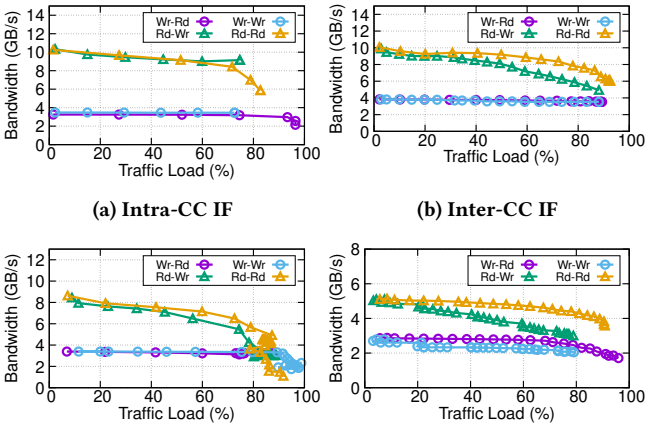
intra-CC queuing module). Bandwidth harvesting does not happen instantly. It takes roughly 100ms and 500ms for the EPYC 9634 to reap unused bandwidth on the IF and P Link, respectively. When flow 0 finishes throttling, the two flows would again take an equal bandwidth share.

When read/write data streams mix, we observe that interference occurs only when a particular link in one direction is saturated. As shown in Figure 6, within a compute chiplet over IF, writes and reads are affected when the background read stream approaches 32.8GB/s and 27.7GB/s. The background write stream induces little interference. Across the compute chiplets, we observe that data stream performance is affected at much higher bandwidth, because the I/O chiplet provisions more than one routing path. For example, the write flow is rarely affected regardless of the background traffic, while reads are degraded when the aggregated bandwidth exceeds 55.7GB/s. At the GMI and P Link/CXL, interference occurs when the aggregated read(write) bandwidth reaches 31.8(29.1) GB/s and 62.8(44.0) GB/s.

Implication #4: Traffic-oblivious bandwidth allocation and routing are the de facto traffic control scheme. This works well for traditional monolithic servers whose NoC bandwidth is over-provisioned. However, this is no longer the case for server chiplet networking, where compute and I/O chiplets might contend for one or several links. Thus, it will be valuable to introduce the communication flow abstraction, materialize it in a global software-based traffic manager, and expose it to the chiplet network. In this way, one could develop application-specialized traffic control instead of relying on the sender side naively. Read and write interference would also occur when an interconnect link in one direction is over-subscribed. Recent studies on host networking [95] offer a promising approach to build upon.

4 Looking Forward

Server chiplet networking changes how processors, memory, and I/O devices communicate across a server platform, entailing unique performance characteristics. We outline new research directions on grappling with its ramifications.



(a) Intra-CC IF (b) Inter-CC IF

(c) GMI (d) P Link/CXL

Figure 6: Read/write interference at the IF, GMI, and P Link/CXL on the EPYC 9634 processor. We run a frontend stream X at max rate, vary the traffic load of the background one Y, and report how much bandwidth X achieves (X-Y).

#1: Hardware-abstracted Chiplet Networking Layer. `Device tree` [21] is a data structure that describes the hardware components and their organizational structure of an embedded/PC/server platform, exposed to the operating system for system management and maintenance. We believe that a similar hardware abstraction for chiplet networks (like `/sys/firmware/chiplet-net`) is essential. It not only presents an architectural overview (as Figure 1), but also provides runtime performance telemetry statistics for each link and intermediate hop through `/proc/chiplet-net`, facilitating low-level system development.

#2: Rethinking Scalable Operating System Design. With hardware modularity, chiplet servers drastically increase the number of cores (e.g., a four-socket AmpereOne server featuring 1024 cores), motivating us to revisit the design principles of many-core operating systems [5, 8, 9, 16]. For example, the multikernel [5] OS structure is motivated by the costly interconnect (i.e., AMD HyperTransport) when handling cache coherence on a shared memory system. It makes inter-core communication explicit and uses asynchronous messages to synchronize replicated states. However, such a design might not be suitable in chiplet networking due to the extended communication path (§3.2), heterogeneous bandwidth domains (§3.3), and inconsistent BDP (§3.4). It is pivotal to explore, refine, or perhaps redefine what the scalable commutative rule [16] is.

#3: Fused Intra-/Inter-Host Networking and I/O Stack. Recent trends indicate that inter-fabric bandwidth has gradually approached or even outpaced intra-host bandwidth, like in disaggregated storage [27, 32, 35, 36, 45, 52–54, 105]. For example, a 400+GbE terabit Ethernet port and 8+ NVMe SSDs

can sometimes drive more bandwidth than a compute chiplet. The problem becomes even worse if considering the inconsistent BDP (§3.4) and unregulated bandwidth partitioning (§3.5). Researchers have partly tackled this issue [13, 32]. For example, NetChannel [13] introduces a disaggregated networking stack and uses a flexible channel abstraction for streaming data in and out. `blk-switch` [32] proposes a switching architecture for the block layer for efficient multi-tenancy. In chiplet networking, the network and I/O stack should consider both the internal and external link characteristics and judiciously orchestrate data flows across compute chiplets, I/O chiplets, memory domains, and devices.

#4: Intra-host Switching for Accelerators. Dense GPU and domain-specific accelerator servers have become prevalent in the era of AI. Although massive data communications use dedicated external fabrics (like NVLink), server chiplet networking is an important component for the signal plane and host-accelerator interaction. Specifically, the accelerator execution is activated via submission commands and completed through acknowledgment responses, which are latency-sensitive. Bandwidth-intensive input/output data is copied to/from the accelerator memory explicitly through DMA or data movement engines, managed by the host CPU. In chiplet networking, all such communications traverse the device bus, I/O hub, and I/O chiplet, which embody performance idiosyncrasies (§3.2–§3.5). To fully utilize the accelerator and eliminate movement-induced stalls, one should develop an intra-host switching module that proactively monitors the traffic matrix [51], conceives an optimal communication path and schedule, and provisions just enough bandwidth. Researchers have explored such a design in programmable networks [7, 14, 22, 42, 75, 76, 83, 84, 104, 106] and in-network computing [29, 44, 46–48, 67, 81].

#5: Chiplet-Centric System Modeling, Benchmarking, and Profiling. Chiplet networking significantly complicates server operational observability, making resource provisioning, performance diagnostics, and debugging challenging. Besides the sub-microsecond granularity, difficulties arise from much more intertwined micro-architectural components, with very limited hardware monitoring counters. We propose to take an interconnect transaction view and develop a chiplet-centric architectural performance model, as many others [2, 19, 26, 43, 101, 102], to capture both data and computing flows. Next, it would be useful to develop a benchmarking framework [30, 60] for cross-platform systematic characterization and to produce practical guidelines. Last, we advocate for a system-level `perf`-like [20, 41] profiling utility, entrenched with the server SoC, that collaboratively combines the hardware architectural PMU (Performance Monitoring Unit) with time-series-based probabilistic and compact data structures (like Sketches [88, 97, 103]) to distill application-specific execution telemetry.

#6: From Server Chiplet Networking to Accelerator Chiplet Networking. As accelerators are increasingly built using chiplets, we believe that accelerator chiplet networking will also be an interesting exploration area. In addition to the idiosyncrasies uncovered in §3, taking existing AI accelerators [70–72, 78, 93, 107] as an example, we expect that (a) the tighter coupling between communication and computation (such as tensor tiles, activation gradient, and attention maps), (b) mixed dataflows (like control-plane kernel dispatching and data-plane tensor streaming), and (c) multi-tier communication hierarchy (e.g., inter-chiplet, on-package NOC, and inter-packet) will impose more challenging issues, requiring us to rethink traffic control, kernel scheduling, and communication collective.

5 Conclusion

This paper introduces a new type of host network–server chiplet networking. We perform a systematic characterization of AMD chiplet-based EPYC server platforms and summarize several key design implications. We outline future research directions, and believe that server chiplet networking will fundamentally shape the design and implementation of future performant, efficient, and scalable server systems.

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